

Docket No. 211134US-2S

IN RE APPLICATION OF: Fumio HIRAHARA, et al.

SERIAL NO: 09/900,946

FILED: July 10, 2001

FOR: SEMICONDUCTOR DEVICE HAVING AT LEAST THREE POWER TERMINALS SUPERPOSED ON EACH OTHER



ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

Transmitted herewith is an amendment in the above-identified application.

- No additional fee is required
 Small entity status of this application under 37 C.F.R. §1.9 and §1.27 is claimed.
 Additional documents filed herewith: Marked-Up Copy

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The Fee has been calculated as shown below:

CLAIMS	CLAIMS REMAINING		HIGHEST NUMBER PREVIOUSLY PAID	NO. EXTRA CLAIMS	RATE	CALCULATIONS
TOTAL	19	MINUS	20	0	x \$18 =	\$0.00
INDEPENDENT	2	MINUS	3	0	x \$84 =	\$0.00
		<input type="checkbox"/> MULTIPLE DEPENDENT CLAIMS		+ \$280 =		\$0.00
						TOTAL OF ABOVE CALCULATIONS \$0.00
		<input type="checkbox"/> Reduction by 50% for filing by Small Entity				\$0.00
		<input type="checkbox"/> Recordation of Assignment		+ \$40 =		\$0.00
						TOTAL \$0.00

- A check in the amount of \$0.00 is attached.
 Please charge any additional Fees for the papers being filed herewith and for which no check is enclosed herewith, or credit any overpayment to deposit Account No. 15-0030. A duplicate copy of this sheet is enclosed.
 If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37 C.F.R. §1.136 for any necessary extension of time may be charged to Deposit Account No. 15-0030. A duplicate copy of this sheet is enclosed.

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211134US-2 S

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF

FUMIO HIRAHARA ET AL

SERIAL NO: 09/900,946

FILED: JULY 10, 2001

FOR: SEMICONDUCTOR DEVICE :
HAVING AT LEAST THREE
POWER TERMINALS SUPERPOSED
ON EACH OTHER

ATENT & TRADEMARK OFFICE

: EXAMINER: MITCHELL, J. M.

: GROUP ART UNIT: 2827

:
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AMENDMENT

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

3/3/03

SIR:

In response to the Official Action mailed October 16, 2002, please amend this application as follows:

IN THE SPECIFICATION

Please amend the specification as follows:¹

Page 1, please replace the paragraph beginning at line 21 to page 2, line 7 as follows:

In FIG. 9A, a collector side of an IGBT chip 65 and an n layer side of a diode chip 66 are soldered respectively, on a Cu pattern 63 of the surface of a DBC (Direct Bond Copper) substrate wherein copper conductors sandwich an insulation substrate 67 of alumina. An emitter side of the IGBT chip 65 and a p layer side of the diode chip 66 are connected with an

¹A marked-up copy of the change made to the specification is attached.